REMARKS

Claims 21-42 are pending in the present application. Claims 1-20 have been canceled. Claims 21-42 have been presented herewith.

Priority Under 35 U.S.C. 119

Applicant notes the Examiner's acknowledgment of the Claim for Priority under 35 U.S.C. 119 and receipt of the certified copy of the priority document.

Drawings

The drawings have been objected to as having insufficient descriptive labels. Accordingly, the drawings have been corrected in a separate Drawing Correction Approval Request filed concurrently herewith. In Figs. 1 and 3-5, the "SELECTORS" have been labeled. Also in Fig. 4, elements 402, 402a and 403 have been denoted respectively as "LOGIC CIRCUIT BLOCK", "LATCH" and "DUMMY LATCH". Corrected formal drawings will be prepared and filed upon approval by the Examiner and subsequent indication of allowance of the present application.

Specification

The disclosure has been objected to in view of the various informalities listed on pages 2-3 of the current Office Action dated December 23, 2002. The specification has been amended to improve form. The Examiner is therefore respectfully requested to

withdraw the objection to the disclosure.

Claim Objections

Claim 1 has been objected to for the reasons stated on page 3 of the Office Action. However, as noted above, claim 1 has been canceled.

Allowable Subject Matter

Applicant respectfully notes the Examiner's acknowledgment that claims 8-11 and 16-19 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form.

Claim Rejections-35 U.S.C. 112

Claim 14 has been rejected under 35 U.S.C. 112, second paragraph, as being indefinite. However, as noted above, claim 14 has been canceled.

Claim Rejections-35 U.S.C. 103

Claims 1-7 and 20 have been rejected under 35 U.S.C. 103(a) as being unpatentable over the Beausang et al. reference (U.S. Patent No. 5,696,771), in view of the Kingsley reference (U.S. Patent No. 6,144,262) and the Kagatani et al. reference (U.S. Patent No. 5,875,114). Also, claims 12, 13 and 15 have been rejected under 35 U.S.C. 103(a) as being unpatentable over the Beausang et al. reference in view of the

Kingsley reference and the Kagatani et al. reference, in further view of the Bassett et al. reference (U.S. Patent No. 4,878,209). These rejections, insofar as they may pertain to the presently pending claims, are traversed for the following reasons.

The semiconductor device of claim 21 includes in combination a fourth signal path "for guiding said test clock, which is input to said clock input terminal, to a fourth pad". Also, "said third and fourth signal paths are formed so that wiring delay time of said third and fourth signal paths are substantially equal". Applicant respectfully submits that the prior art as relied upon by the Examiner does not make obvious these features.

The semiconductor device of the present invention can remove the influence of signal path delay, when an access time of the circuit block is measured. As described with respect to Figs. 1 and 2 of the present application, a circuit block 101 has input thereto an input signal D at a timing when a clock CLK rises to a high level. In other words, an input signal D is applied to the block 101 before a timing when the clock CLK rises, and the input signal D is read by block 101 when the clock CLK rises to a high level from a low level. After this, circuit block 101 outputs an output signal Q. In this case, access time means the time lag from when signal D is input to block 101 until signal Q is output, that is the time from when clock CLK rises to a high level until signal Q is output. In the case where a signal path is not provided between an output of selector 103 and selector 105 to pad 110, an access time is detected by measuring a

time lag from when a test clock TCLK is applied to pad 108 until when a test signal TQ is output to pad 109. However, this method cannot measure an access time exactly, because the time delay from pad 108 to block 101 and the time delay from block 101 to pad 109 are contained in the result of the measurement.

On the other hand, an access time can be measured exactly in the semiconductor device of claim 21. The semiconductor device of claim 21 includes a fourth signal path, and thus can output the test clock which is input to the circuit block as an output via a fourth pad. That is, the test clock is output from the fourth pad via the fourth signal path after being input to the circuit block. The time lag from when a test clock is input to the second pad until when the test clock is output to the fourth pad, contains the time delay from the second pad to the circuit block and the time delay from the circuit block to the fourth pad. Here, the wiring delay time of the third and fourth signal paths are substantially equal. Therefore, time delay from the circuit block to the third pad, and time delay from the circuit block to the fourth pad, are substantially the same. As a result, the time lag from when a test clock is input to the second pad until when a test clock is output to the fourth pad (that is, T2 in Fig. 2) is the same as the total of the time delay from the second pad to the circuit block (that is, T1 in Fig. 2) and the time delay from the circuit block to the third pad (that is, t2 in Fig. 2). Consequently, the semiconductor device can measure an access time exactly by subtracting a measured time lag T2 from a measured time lag from when a test clock is applied to the second pad until when a signal is output via the third pad (that is, T1 in Fig. 2).

Applicant respectfully submits that the prior art as relied upon by the Examiner does not particularly disclose third and fourth signal paths as featured in claim 21 and as described above, and more particularly does not feature third and fourth signal pads that "are formed so that wiring delay time of said third and fourth signal paths are substantially equal". Accordingly, Applicant respectfully submits that the semiconductor device of claim 21 would not have been obvious in view of the prior art as relied upon by the Examiner taken singularly or together, and that this rejection, insofar as it may pertain to claims 21-25, is improper for at least these reasons.

The semiconductor device of claim 26 includes in combination a third signal path "for guiding a test output signal, which has been output from a signal output terminal of said circuit block", a fourth signal path "for guiding said test clock, which is input to said clock input terminal", and a selector "which selectively supplies said test output signal from said third signal path or said test clock from said fourth signal path to a third pad". Applicant respectfully submits that the various prior art as relied upon by the Examiner does not disclose or make obvious these features.

Particularly, the prior art as relied upon by the Examiner does not specifically disclose a selector provided in connection with signal paths of a circuit block to provide a signal to a pad. More particularly, the prior art as relied upon by the Examiner does not disclose or even remotely suggest a selector which selectively supplies a test output signal of a circuit block, or a test clock input to the circuit block, to a pad. Figs. 5A-5D of the Beausang et al. reference merely disclose selector 430 at a data input stage of

the memory cells 450. The Kinglsey and Kagatani et al. references as relied upon by the Examiner do not specifically appear to disclose selectors. Also, the Bassett et al. reference as secondarily relied upon by the Examiner does not specifically disclose a selector.

Accordingly, Applicant respectfully submits that the semiconductor device of claim 26 would not have been obvious in view of the prior art as relied upon by the Examiner taken singularly or together, and that the above noted rejections, insofar as they may pertain to claims 26-30, are improper for at least these reasons. Applicant also respectfully asserts that claim 26 includes somewhat similar features as original claim 8, which has been acknowledged by the Examiner as including allowable subject matter. Accordingly, claims 26-30 should thus distinguish over the relied upon prior art for at least these additional reasons.

The semiconductor device of claim 31 includes in combination a third signal path "for guiding a test output signal, which has been output from a signal output terminal of said circuit block, to a third pad via a dummy latch". The dummy latch is featured as constituted so as to "latch said test output signal at substantially a same operating speed as an operational latch for latching an output signal of said circuit block during a normal operation". Also, the third signal path is featured as "formed so that a wiring delay time from said signal output terminal of said circuit block to said dummy latch is substantially equal to a wiring delay time from said signal output terminal of said circuit

block to said operational latch". Applicant respectfully submits that the prior art as relied upon by the Examiner does not disclose or make obvious these features.

The Examiner has apparently interpreted TS latch 12 in Fig. 1 of the Bassett et al. reference as a dummy latch. However, as described in column 3, lines 53-54 of the Bassett et al. reference, latch 12 is designed so that it supplies macro-select signal MS to the test out line when test strobe TS is "HIGH". Latch 12 of the Bassett et al. reference thus does not provide a test output signal from a circuit block to an output pad, but merely provides a macro-select signal. More particularly, latch 12 of the Bassett et al. reference is not disclosed or even remotely suggested as having substantially a same operating speed as an operational latch for latching an output signal of a circuit block during a normal operation. Additionally, the Bassett et al. reference does not disclose or even remotely suggest a third signal path formed wherein a wiring delay time from a signal output terminal of a circuit block to a dummy latch is substantially equal to a wiring delay time from the signal output terminal of the circuit block to an operational latch. Accordingly, Applicant respectfully submits that the semiconductor device of claim 31 would not have been obvious in view of the prior art as relied upon by the Examiner taken singularly or together, and that the above noted rejections, insofar as they may pertain to claims 31-35, are improper for at least these reasons.

The semiconductor device of claim 36 includes in combination a second signal path "for guiding a test clock, which has been supplied to a second pad, to a clock input

terminal of said circuit block", a third signal path "for guiding a test output signal, which has been output from a signal output terminal of said circuit block, to a third pad" and a fourth signal path "for selectively guiding said test clock input to said clock input terminal of said circuit block, and said test input signal input to said signal input terminal of said circuit block, as an output of the semiconductor device". Applicant respectfully submits that the prior art as relied upon by the Examiner does not disclose or make obvious these features.

As emphasized previously, only the Beausang et al. reference as specifically relied upon by the Examiner discloses a selector. However, selectors 430 in Figs. 5B and 5D of the Beausang et al. reference are merely provided at data input stages of the memory cells. The prior art as relied upon by the Examiner does not specifically disclose or even remotely suggest selectively providing a test clock input to a clock input terminal of a circuit block and a test input signal input to a signal input terminal of a circuit block, as an output of a semiconductor device. Accordingly, Applicant respectfully submits that the semiconductor device of claim 36 would not have been obvious in view of the prior art as relied upon by the Examiner taken singularly or together, and that these above noted rejections, insofar as they may pertain to claims 36-42, are improper for at least these reasons.

Conclusion

The Examiner is respectfully requested to reconsider and withdraw the corresponding rejections, and to pass the claims of the present application to issue, for at least the above reasons.

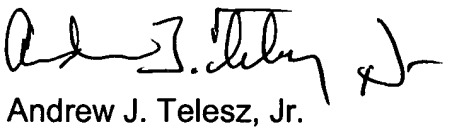
In the event that there are any outstanding matters remaining in the present application, please contact Andrew J. Telesz, Jr. (Reg. No. 33,581) at (703) 715-0870 in the Washington, D.C. area, to discuss these matters.

Pursuant to the provisions of 37 C.F.R. 1.17 and 1.136(a), the Applicant hereby petitions for an extension of one (1) month to April 23, 2003, for the period in which to file a response to the outstanding Office Action. The required fee of $110.00 is attached hereto.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 50-0238 for any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17; particularly, extension of time fees.

Respectfully submitted,

VOLENTINE FRANCOS, P.L.L.C.



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Enclosures: Version with Marked-Up Changes

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VERSION WITH MARKED-UP CHANGES

Additions/Deletions to the Abstract:

[This] A semiconductor device [comprises:] including a first signal path for guiding [the] an input signal from a first pad to [the] an input terminal of [the] a macro cell; a second signal path for guiding [the] a clock from a second pad to [the] a clock input terminal of the macro cell; a third signal path for guiding [a] an output signal from [the] a signal output terminal of the macro cell to a third pad; and a [forth] fourth signal path for receiving the clock from the first signal path and guiding the clock to a fourth pad. It is possible to eliminate [the] wiring delay by measuring the time from when the input signal and the clock are supplied by the first and second [pad] pads until the output signal is output by the third pad, and the time from when the clock is supplied to the second path until it is output by the fourth pad.

Additions/Deletions to the Specification:

Page 5, lines 4-10:

The preferred embodiments of the present invention are explained below using the drawings. In the drawings, the sizes, forms, and positional relationships of the various constitutional elements are only shown in general so that the invention can be easily understood. Also, the numerical conditions explained below are merely examples to make the invention [understand] understandable.

Page 8, lines 8-22:

When performing a functional test, the signal TEST supplied to the pad 106 is set to the signal value for the functional test mode. As a result, the multiplexer 102 selects the pad 107, the multiplexer 103 selects the pad 108, the multiplexer 104 selects the signal Q, and the multiplexer 105 selects the clock CLK. Next, the test signal TD is input from the pad 107 and the test clock TCLK is input from the pad 108. The test signal TD and test clock TCLK are input to the macro cell 101 through the multiplexers 102 and 103. The macro cell 101 then reads the test signal TD at the time indicated by the test clock TCLK (rise time in the example in Figure 2), and outputs the signal Q of a value corresponding to the value of this test signal TD. This signal [Q] TQ is output from the pad 109 through the multiplexer 104. Also, the test clock TCLK is output as a clock MCLK from the pad 110 through the multiplexer 105.

Page 8, line 23 through to page 9, line 15:

In the present embodiment, the required time T1 from when the test clock TCLK is supplied to the pad 108 until the pad 109 outputs the signal [Q] TQ and the required time T2 from when the test clock TCLK is supplied to the pad 108 until the pad 110 outputs the test clock MCLK are measured. The difference between these required times T1-T2 is then calculated. As shown in Figure 2, when the time from when the test clock TCLK is applied to the pad 108 until the test clock TCLK is input to the macro cell 101 is t1; the time from when the macro cell receives the test clock TCLK until the macro cell outputs the signal Q (meaning access time) is tx; and the time from when the

signal Q is output until this signal Q reaches the pad 109 is t2, then the time T1 = t1 + tx + t2. Also, as discussed above, the wiring delay from the output terminal Q to the pad 109 and wiring delay from the clock input terminal CLK to the pad 110 are substantially the same and therefore the time T2 = t1 + t2. Consequently, the time difference T1-T2 matches the access time tx. In other words, the time difference T1-T2 is the value obtained by removing the effect of the wiring delay from the measured value of the access time T1.

Page 15, line 24 through to page 16, line 8:

In the case of performing a functional test, the signal TEST supplied to the pad 408 is set at the signal value for the functional test mode. As a result, the multiplexer 404 selects the pad 409, the multiplexer 405 selects the pad 410, the multiplexer 406 selects the signal Q, and the multiplexer 407 selects the output signal of the latch 403. The test signal TD and test clock TCLK are input to the macro cell 401 through the multiplexers 404 and 405. The macro cell 401 then outputs the signal Q. This signal [Q] TQ is output from the pad 412 through the multiplexer 406. Also, this signal Q is held in the latch 403. The signal Tq held in the latch 403 is output from the pad 411 through the multiplexer 407.

Page 19, lines 4-25:

When performing a functional test, the signal TEST supplied to the pad 507 is set at a signal value for the functional test mode. Furthermore, the signal MODE

supplied to the pad 506 is set at a signal value for selecting the signal input terminal D. As a result, the multiplexer 502 selects the pad 508, the multiplexer 503 selects the pad 509, the multiplexer 504 selects the signal Q, and the multiplexer 505 selects the signal input terminal D. The test signal TD is then input from the pad 508 and the test clock TCLK is input from the pad 509. At this time, after a prescribed period of time t1 from when the test signal TD is applied to the pad 508, the test clock TCLK rises and then after a prescribed period of time t2 from this rise time, the application of the test signal TD ends. These signals TD and TCLK are applied to the macro cell 501 through the multiplexers 502 and 503. The macro cell 501 receives the test signal TD at the rise time of the test clock TCLK and outputs the signal Q of a value corresponding to the value of this signal TD. This signal [Q] TQ is output from the pad 510 through the multiplexer 504. Also, the signal [D] TD is output from the pad 511 [to] through the multiplexer 505. At this time, the required time T7, from when the test signal TD is supplied to the pad 508 until the pad [510] 511 outputs the signal TD [D], is measured.

Page 19, line 26 through to page 20, line 4:

Next, the signal MODE is converted to the signal value for selecting the clock input terminal CLK. At this time, the test clock TCLK is input from the pad 509 [508]. The test clock TCLK is output from the pad 511 through the multiplexers 503 and 505. The required time T8 from when the test clock TCLK is supplied to the pad 509 until the pad 511 outputs the test clock TCLK is measured.